TMS9918 EXTERNAL VIDEO CIRCUIT

ABSTRACT - This report briefly describes a circuit for synchronizing a TMS9918 Video Display Processor (VDP) to a standard NTSC broadcast signal. This report assumes the reader has some knowledge of T.V. signals and is familiar with the VDP. At the end of this report, some limitations of the circuit are given.

THE CIRCUIT (Refer to figure 1)

A standard NTSC broadcast signal is applied to the external video of the circuit. A General Electric ECG 1064 is used as the heart of the SYNC stripper circuit, an ECG 1132 (gated phase lock loop) was used for the subcarrier regenerator, and a 74LS221 was used to generate the burst window.

The function of the SYNC stripper circuit is to separate out the SYNC part (both horizontal and vertical) of the T.V. signal. External video is A.C. coupled and D.C. biased via a 15uf capacitor and 10K pot on the input 10 of the ECG 1064. The output on pin 16 is a roughly 10 volt peak to peak SYNC signal.

The output of the SYNC stripper is fed to a bootstrap type level shifter. The VDP uses a combined SYNC/reset pin where reset is 0 volts and SYNC is about 10 volts and neither is nominally 5 volts. The 1.2K resistor of the SYNC circuit maintains a D.C. 5 volt level. A switch, or the like can be used to pull the output to ground thus invoking reset. The composite SYNC signal is capacitively coupled to SYNC level shifter so that when the composite SYNC signal goes from 0 to 10 volts the level shifter is bootstrapped from +5 to 12 volts via the 100uf capacitor (the exact value of this capacitor is not important so long as it is "much greater" than 20pf nominal on the output of the level shifter); the 1N4742A is used to voltage limit the output to 12 volts so as to prevent excessive voltage going to the VDP (note that without the diode the voltage could get to about 15 volts) . The output of the level shifter circuit is directly connected to the VDP reset/SYNC pin.

The burst window generator is used to indicate where the burst signal occurs for controlling the gated phase lock loop in the subcarrier regenerator (see figure 2 for burst window). There are 2 one shots in this circuit. The first one shot generates the delay from the horizontal SYNC to the start of the burst window (the 10K trim pot is used to exactly tune this delay). The first one shot triggers, the second one shot to fire; the pulse width (or burst window) of the second one shot is set by a 8.2K resistor and a 1200pf capacitor.

The burst window generator output is D.C. level shifted by 2 volts for feeding to the subcarrier regenerator. The ECG 1132 gate phase lock loop samples the external video in and locks to it when the input 9 (the burst window) indicates. The output of the phase lock loop is a 3.58 signal with a fix phase relationship to the burst frequency of the T.V. signal. The 3.58 signal is buffered and fed to a 3rd harmonic circuit to get the 10.7 clock

input for the VDP. (Note, since T.V. depends on the phase relationship to the burst frequency the phase delay between external video in and the VDP's clock input controls the tint. An optional phase delay circuit can be used to control the "tint" of the VDP's colors). The 3rd harmonic circuit is "tuned" by a 1.5 to .8 uh coil/transformer. The buffered output of the 3rd harmonic circuit drives the VDP's input clock.

The external video signal must be A.C. and D.C. adjusted to the external video input of the VDP in order to obtain proper SYNC and luminance levels on the composite video output of the VDP.

NOTES AND CAUTIONS

- The circuit described has not been thoroughly checked and tested for reliability given any composite video input.

- There is some "dot crawl" or "zipper effect" in the picture. This is because the synchronization inside the VDP in only at the dot display rate, and therefore, there can be a 1 dot synchronization error. While the crawl is noticable, a very readable text can be displayed.

- Because there is a divide by three of the input clock frequency to get the color phase generator inside the VDP, the VDP can be in one of three phase relationships with respect to the external video signal. For example, if the T.V. signal is interrupted so that the subcarrier regenerator must "relock", what was a red square on the screen drawn by the VDP may come up blue the next time. The solution to this problem has not been worked out at this time.

- The dot crawl or zipper effect can theoretically be reduced by external circuitry if color lock is not important. (Note: it is impossible with the current VDP to get both color lock and no zipper effect), however, we have not developed and built a circuit to do this yet.

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Figure 1

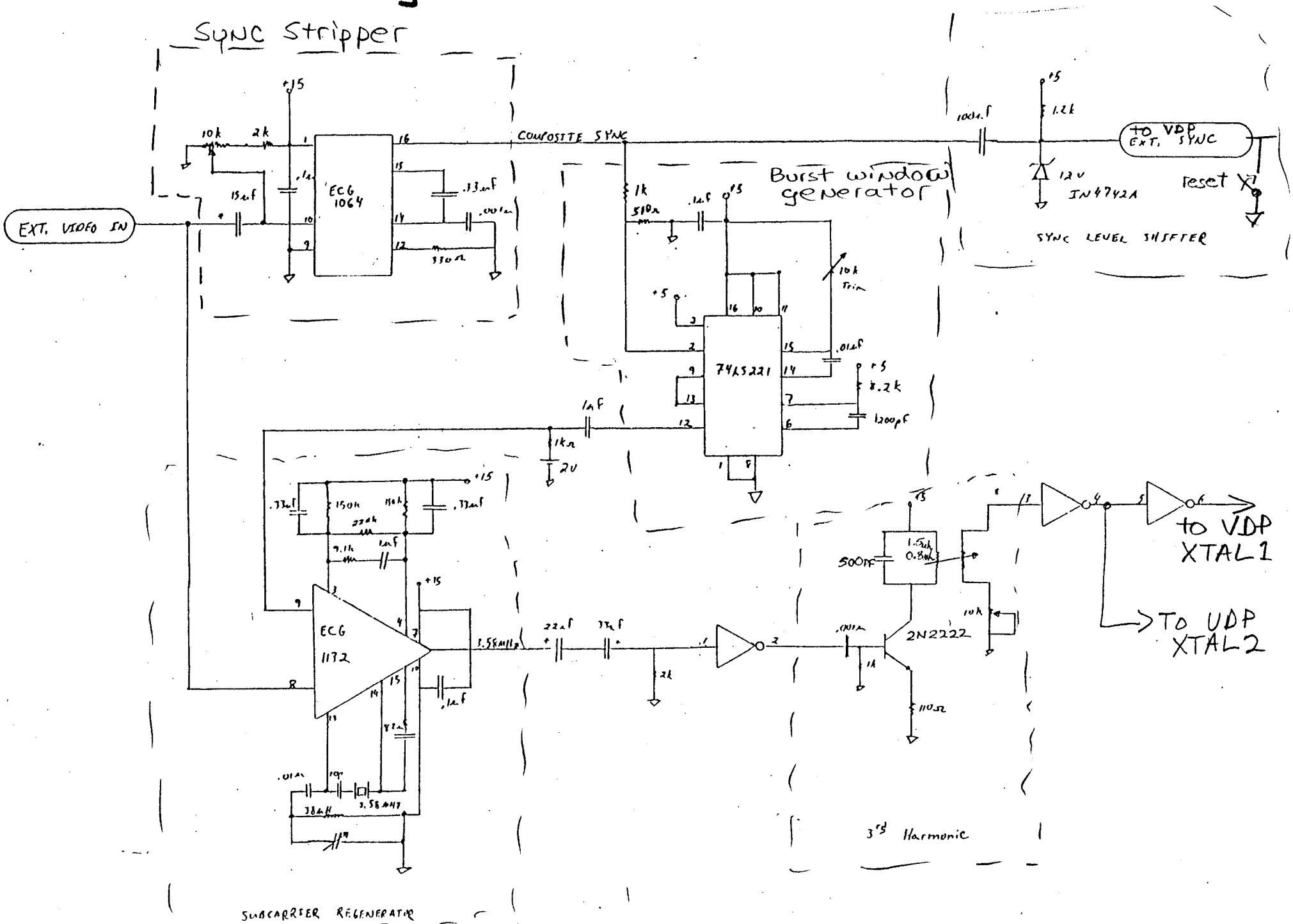
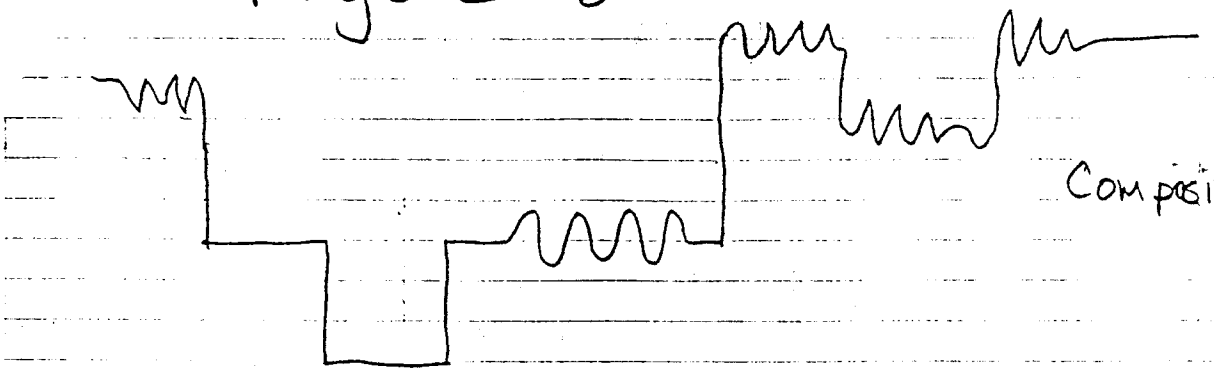
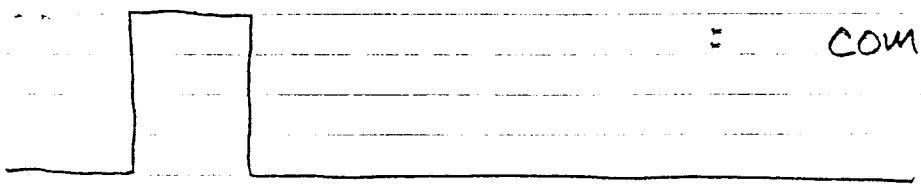


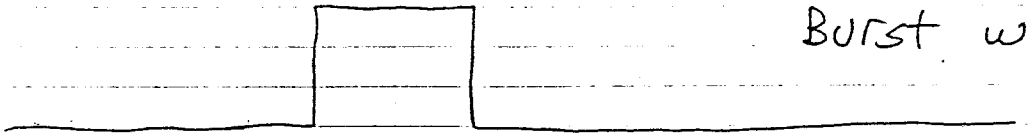
Figure 2



Composite video



: composite sync.



Burst window